Remarks/Arguments

This Amendment is in response to the Final Office Action mailed 07 July 2005. Specifically, the Examiner rejected claims 44, 45, and 46 under 35 USC 112, 2nd paragraph as being indefinite. Additionally, the Examiner rejected claims 44, 45, and 46 under 35 USC 101 as the claimed invention is directed to non-statutory subject matter. Further, the Examiner rejected claims 41, 42, and 43 under 35 USC 102(a) as being anticipated by Palmchip Product Brief PALM-DP-2000 "AcurX Configurable SoC Platform" (DP-2000). Further, the Examiner rejected claims 41, 42, 43, 45, and 46 under 35 USC 103(a) as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089), Applicant Admitted Prior Art (AAPA), and LaBerge (US Patent No. 6,513,089). Additionally, the Examiner rejected claim 44 as being unpatentable under 35 USC 103(a) over Hoffman, AAPA, and LaBerge, in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), and Pawlowski et al. (US Patent No. 5,469,547). Further, the Examiner rejected claims 41, 42, and 43 under 35 USC 103(a) as being unpatentable over Hoffman, LaBerge, and Jou et al. (US Patent No. 6594814). Finally, the Examiner rejected Applicant's claim for domestic priority under 35 USC 119(e) as the provisional applications fail to provide adequate support under 35 USC 112 for claims 41 – 46.

1. Summary of Current Claims

Claims 41-43 are currently amended. And, claims 44-46 have been canceled.

2. Rejection under 35 USC 112, 2nd paragraph

The Examiner rejected claims 44, 45, and 46 under 35 USC 112, 2nd paragraph as being indefinite. The Applicant has canceled claims 44-46 and moved those dependent claims into the corresponding independent claims. Therefore, the Applicant requests that the Examiner withdraw the rejection to claims 44, 45, and 46 under 35 USC 112, 2nd paragraph as being indefinite.

3. Rejection under 35 USC 101

The Examiner rejected claims 44, 45, and 46 under 35 USC 101 as the claimed invention is directed to non-statutory subject matter. The Applicant has canceled claims 44-46 and moved those dependent claims into the corresponding independent claims. Therefore, the Applicant requests that the Examiner withdraw the rejection to claims 44, 45, and 46 under 35 USC 101 as the claimed invention is directed to non-statutory subject matter.

4. Rejection under 35 USC 102

The Examiner rejected claims 41, 42, and 43 under 35 USC 102(a) as being anticipated by Palmchip Product Brief PALM-DP-2000 "AcurX Configurable SoC Platform" (DP-2000). The publication date for this reference as listed on its first page is October 2002. The parent application of the instant application, App. Ser. No. 10/180,866, was filed on 26 July 2002. The parent application was filed several months before the publication of the cited reference. Thus, the cited reference is not a valid 102(a) reference. Therefore, the Applicant requests that the Examiner withdraw the

rejection to claims 41, 42, and 43 under 35 USC 102(a) as being anticipated by Palmchip Product Brief PALM-DP-2000 "AcurX Configurable SoC Platform" (DP-2000).

5. Applicant Admitted Prior Art

In the Office Action , the Examiner maintained the determination regarding Applicant Admitted Prior Art. The only response that the Examiner can muster to the Applicant's prior response is the following: "Further, as the Applicant has pointed out on Page 9 of the arguments, Paragraphs 9 and 12 describe the problems solved by the present invention, and thus disclose a previously known method of using pipeline stages in an SOC device." The Applicant disagrees with the Examiner's position because essentially the Examiner's argument is that the claimed invention and the solution solved by the claimed invention render the claimed invention either anticipated or obvious in view of its own disclosure. If the only prior disclosure of the claimed invention is the claimed invention's disclosure, then the claimed invention must, by definition, is novel and non-obvious over the prior art.

The Examiner's response does not address the Applicant's response, specifically the following:

> Specifically, the Examiner made the determination that the specification, p. 4, l. 15-23 and p. 6, l. 19 - p. 7, l. 2 teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any single initiator and any signal target. Additionally, the Examiner made the determination that the specification, p. 5, l. 9 -12 and p. 6, l. 19 - p. 7, l. 2 teaches that the coupling of the first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning a single integrated circuit.

PAGE 12/19 * RCVD AT 1/7/2006 2:43:29 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:512-474-7996 * DURATION (mm-ss):11-24

As in the prior response, the Examiner is unable to cite a specific reference that contains these novel elements. Rather, the Examiner as before, is using the Applicant's novel disclosure against itself to arrive at his determination.

The Applicant again respectfully requests that the Examiner withdraw the original determination regarding Applicant Admitted Prior Art.

6. Claim Rejection under 35 USC 103(a)

The Examiner rejected claims 41, 42, 43, 45, and 46 under 35 USC 103(a) as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089), Applicant Admitted Prior Art (AAPA), and LaBerge (US Patent No. 6,513,089). In response to the Office Action, Applicant is amending and reordering the claims to further clarify the claimed invention. Applicant believes that these amendments place the pending claims in immediate condition for allowance or appeal.

The Applicant reasserts that the Examiner has failed to make a prima facie case of obviousness. Additionally, the Applicant reasserts that Hoffman and LaBerge are not proper 103(a) references. And more specifically, the Applicant reasserts that the Examiner failed to create Applicant Admitted Prior Art (AAPA). Without the AAPA as a reference, the Examiner is unable to make a prima facie rejection relying on Hoffman and LaBerge alone.

In support of the Examiner's rejection, the Examiner finds the following with regard to Hofmann:

> Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number

> of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration.

The recited elements go to the heart of the claimed invention. The Examiner admits that Hofmann does not anticipate or teach these elements. Yet, the Examiner is unable to find these elements in Hofmann or LaBerge. The only reference that the Examiner is citing where these elements are found or taught is the Applicant's own disclosure. The Examiner is saying on one hand that the claimed invention is novel and non-obvious because he is unable to find a reference that anticipates or teaches the above claim limitations; and at the same time, the Examiner is saying that the Applicant's own novel and non-obvious disclosure of those elements renders the claimed invention obvious. The Examiner cannot have this issue both ways.

The Applicant therefore respectfully requests that the Examiner withdraw the rejections to claims 41, 42, 43, 45, and 46 under 35 USC 103(a) as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089), Applicant Admitted Prior Art (AAPA), and LaBerge (US Patent No. 6,513,089).

The Examiner additionally rejected claim 44 as being unpatentable under 35 USC 103(a) over Hoffman, AAPA, and LaBerge, in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), and Pawlowski et al. (US Patent No. 5,469,547). As previously discussed, the failure of non-existent AAPA, Hoffman, and LaBerge not teaching or suggesting all of the claim elements and limitations of the claimed invention either individually or in combination means that

these are not proper 103(a) references, and thus when combined with Sheafor, Quereshi, and Pawlowski still do not make a prima facie case for obviousness. Applicant therefore respectfully requests that the Examiner withdraw the rejections to claim 44 as being unpatentable under 35 USC 103(a) over Hoffman, AAPA, and LaBerge, in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), and Pawlowski et al. (US Patent No. 5,469,547).

7. Claim Rejection under 35 USC 103(a)

The Examiner additionally rejected claims 41, 42, and 43 under 35 USC 103(a) as being unpatentable over Hoffman, LaBerge, and Jou et al. (US Patent No. 6594814).

In support of the Examiner's rejection, the Examiner finds the following with regard to Hofmann:

> Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration.

The recited elements go to the heart of the claimed invention. The Examiner admits that Hofmann does not anticipate or teach these elements. Yet, the Examiner is unable to find these elements in Hofman, LaBerge or the newly cited reference Jou. The only reference that the Examiner cites in a back door fashion where these elements are found or taught is the Applicant's own disclosure. The Examiner is saying on one hand

that the claimed invention is novel and non-obvious because he is unable to find a reference that anticipates or teaches the above claim limitations; and at the same time, the Examiner is saying that the Applicant's own novel and non-obvious disclosure of those elements renders the claimed invention obvious. The Examiner cannot have this issue both ways.

The Examiner states that Jou "teaches that the use of pipelining is well-known in integrated circuit design (See Abstract) and the use of pipelines having a dynamically variable number of stages (See Column 1 lines 55-58 and Column 2 lines 12-17)." As a reference, Jou neither adds to or subtracts from the Examiner's use of Hofmann or LaBerge. The Examiner actually has to reference his determination of AAPA to show the above elements that he admits that Hofmann does not disclose or teach. In other words, the Examiner is having to use his determination of AAPA for this rejection, thus this rejection really includes his determination of AAPA.

Therefore, the Examiner has failed to establish a prima facie case of obviousness for Hoffman, LaBerge, Jou, and the backhanded use of the non-existent AAPA, or their combination as 103(a) references. To establish a prima facie case of obviousness, an Examiner must met 3 basic criteria:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
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> MPEP 2143.

PAGE 16/19 * RCVD AT 1/7/2006 2:43:29 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:512-474-7996 * DURATION (mm-ss):11-24

When an Examiner is applying 35 USC 103, the Examiner must consider and follow the following standards:

> When applying 35 USC 103, the following tenets of patent law must be adhered to:
> (A) The claimed invention must be considered as a whole;
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and
> (D) Reasonable expectation of success is the standard with which obviousness is determined.
>
> MPEP 2141

The Examiner has not considered the claimed invention as a whole. Additionally, the Examiner has failed to consider all elements and limitations of Applicant's claims. This results in the failure Hoffman, LaBerge, Jou, and the non-existent AAPA, not teaching or suggesting all of the claim elements and limitations of the claimed invention either individually or in combination. Principally, none of the cited references, either alone or in combination teach an SOC design architecture with a latency tolerant signal protocol that carries signals from signal initiators to signal targets in an SOC where the latency tolerant signal protocol provides for an arbitrary number of pipeline stages between any signal initiator and any signal target where the arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration.

Since the present claims include elements and limitations that are not shown, taught, or implied by the prior art, Applicant therefore respectfully requests that the Examiner withdraw the rejections to claims 41, 42, and 43 under 35 USC 103(a) as being unpatentable over Hoffman, LaBerge, and Jou et al. (US Patent No. 6594814).

8. Claim of Priority

The Examiner additionally rejected Applicant's claim for domestic priority under 35 USC 119(e) as the provisional applications fail to provide adequate support under 35 USC 112 for claims 41 – 46.

Provisional App. Ser. No. 60/390,501, filed on 06-21-2002, provides support for all of the claimed elements including the latency tolerant signal protocol and the arbitrary number of pipeline stages at during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. Support for these and other claimed elements can be found generally throughout the entire provisional specification and can be found in more detail at pp. 25-32 and pp. 41-58 of the provisional specification.

Provisional App. Ser. No. 60/300,709, filed on 06-26-2001, provides support for all of the claimed elements including the latency tolerant signal protocol and the arbitrary number of pipeline stages at during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. Support for these and other claimed elements can be found generally throughout the entire provisional specification and can be found in more detail at pp. 6-12 of the provisional specification.

The Applicant therefore respectfully requests that the Examiner withdraw the rejections to Applicant's claim for domestic priority under 35 USC 119(e) as the provisional applications fail to provide adequate support under 35 USC 112 for claims 41 – 46.

9. Summary

In view of the above, Applicant believes that each of the presently pending claims is in immediate condition for allowance or appeal. Accordingly, Applicant respectfully requests that the Examiner withdraw the outstanding objections and rejections of the claims and issue a timely Notice of Allowance in this case.

Respectfully submitted,
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PAGE 19/19 * RCVD AT 1/7/2006 2:43:29 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:512-474-7996 * DURATION (mm-ss):11-24